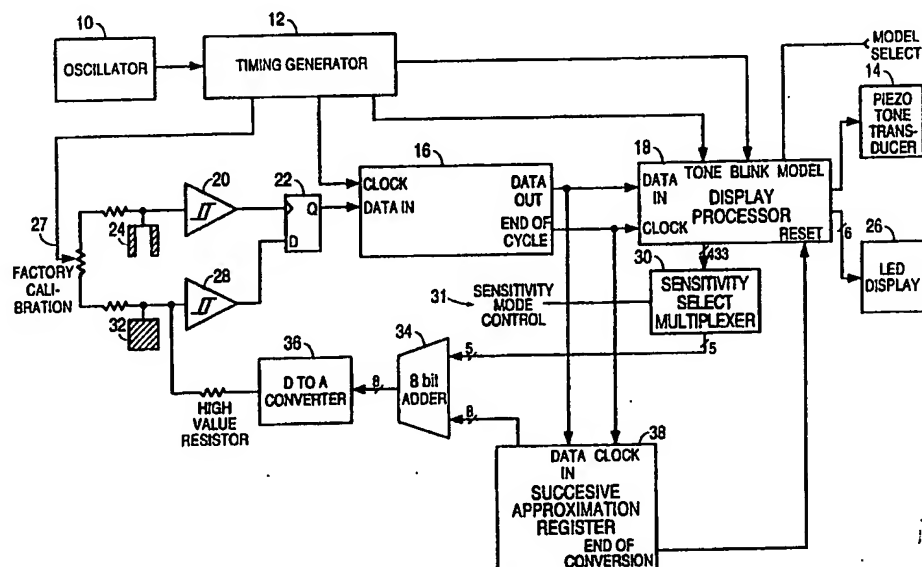


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(54) Title: DUAL SENSITIVITY STUD SENSOR**(57) Abstract**

A dual sensitivity stud sensor senses studs through both thick and thin surfaces. Studs are sensed by detecting a change in the capacitive loading of plates (24, 32) as they are moved along a surface and in proximity with a stud. The sensor informs the operator, via output (14, 18, 26), when the sensor has been incorrectly calibrated over a stud. The sensor also informs the operator if the sensor is placed against a surface either too thick or too thin for stud detection. Through use of a digital register (38), the sensor remains calibrated indefinitely while the sensor is powered on.

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DUAL SENSITIVITY STUD SENSOR

BACKGROUND OF THE INVENTIONField of the Invention

5 This invention relates to an electronic sensor, and, in particular, to a sensor suitable for detecting the location of studs behind a variety of surfaces, including walls, floors and similar type structures. More specifically, the invention relates to an electronic stud
10 sensor with two sensitivity modes for determining the location of studs behind either thick or thin surfaces, and with the ability to inform the user when the sensor has been calibrated over a stud.

Description of the Prior Art

15 U.S. Pat. No. 4,464,622 issued Aug. 7, 1984, and incorporated by reference herein, discloses an electronic wall stud sensor particularly suitable for locating a wall stud positioned behind a wall surface. The sensor detects the stud by measuring a change in the capacitance of the
20 wall due to the presence of a stud while the sensor is moved along the wall surface. The sensor includes a plurality of capacitor plates mounted in the sensor close to the wall surface, a circuit for detecting any changes in the capacitance of the capacitor plates due to a change
25 in the dielectric constant of the wall caused by the location of a stud positioned behind the wall surface and immediately adjacent to the capacitor, and an indicator for indicating the change in capacitance of the capacitor plate, thereby indicating the wall stud position. The
30 sensor also alerts the operator when calibration is occurring.

While the above described electronic wall stud sensor operates as described to locate studs in walls, experience has shown that its performance could be improved in

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several respects. The stud sensor is unable to reliably sense studs through surfaces significantly thicker than the typical 5/8 inch sheetrock wall. For instance, the sensor can not sense floor joists (another type of stud) under a combination of 3/4 inch subfloor and 1/4 inch oak flooring.

Moreover, the stud sensor is incapable of informing the operator when the sensor has been calibrated over a stud. When the sensor is subsequently moved from the stud after completion of this incorrect calibration, it is unable to detect studs and no indication is given that the sensor was incorrectly calibrated. Finally, the stud sensor's correct calibration voltage has a tendency to "leak off," due to use of a sample-and-hold capacitor. This results in less accurate readings after approximately a minute of use.

Therefore, there is a need to sense studs through both thick and thin surfaces. There is also a need to determine when the device has been calibrated over a stud, and informing the operator of this. Further, there is a need for a circuit which maintains calibration indefinitely.

SUMMARY OF THE INVENTION

In accordance with the present invention, a dual sensitivity stud sensor senses studs through both thick and thin surfaces. The sensor also has the ability to sense both an increase and a decrease in density. This allows the device to inform the user when the sensor has been incorrectly calibrated over a stud. Further, the device will notify the operator when the surface being sensed is either too thick or too thin for stud detection. By use of a digital register to store calibration data, calibration is maintained indefinitely while the stud sensor is powered on.

Finally, through use of a tri-state driver and a D type flip-flop, a single IC pin of the stud sensor

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circuitry is employed as both an input and an output, and becomes, in effect, a bi-directional port.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an embodiment of the invention.

Figure 2 shows various waveforms of the sensing portion of the circuit of FIG. 1.

Figure 3 is a schematic of a circuit allowing both input to and output from a single pin of an integrated circuit.

Figure 4 is a schematic showing the capacitive memory for keeping track of the time at which the stud sensor is powered up.

DETAILED DESCRIPTION OF THE INVENTION

15 Operation

Shown in FIG. 1 is an embodiment of the invention for locating positions of studs behind a surface through capacitive sensing.

As in the prior art patent referenced above, operation of this circuit detects the change in capacitive loading of the sensor plates 24 and 32 as they are moved along a surface and into proximity with a stud. Plate 32 is positioned between a pair of coupled plates 24 in the same manner as the plates in the prior art. Schmitt triggers 20 and 28 function in the same manner as the one shot multi-vibrators described in the prior art patent. Therefore, as in the prior art patent, additional capacitive loading due to the presence of a stud unbalances a differential capacitive plate circuit.

However, in accordance with one feature of this invention, the unbalance is traced via a counter in the display processor 18 which injects an offset voltage into the sensor plate circuit via a digital-to-analog (D/A) converter 36. Each step of the counter corresponds to a unique voltage step certain steps of which are also

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associated with a particular LED in the LED display 26.

As additional capacitive loading occurs due to the stud density, the LEDs in LED display 26 correspondingly change, signaling the stud's presence. The unit is
5 calibrated such that the top LED illuminates as the unit is directly over the edge of a stud, with intermediate LEDs showing the approach to the stud's edge. A tone output from the piezo electric tone transducer 14 occurs concurrent with the illumination of the top LED of the LED
10 display 26.

The capacitive null of the sensor plates, i.e., when each sensor plate is equally "loaded," is also sensed through the Schmitt triggers 20 and 28. As shown in FIG. 2, the outputs from these Schmitt triggers then drive
15 respectively the clock input 58 and data input 60 of a D type flip-flop 22. If the plates are unequally "loaded," either the clock input 58 or the data input 60 to the flip-flop 22 will occur first, setting the output 62 of the flip-flop to either a one or a zero. A null, or
20 balanced differential plate capacitance state, is detected by increasing, in small incremental steps, via the digital-to-analog (D/A) converter 36, the offset injection voltage to the sensor plate circuit until the output 62 of the flip-flop 22 changes state. This signals
25 a null condition.

As also shown in FIG. 2, the sensor plate circuit is driven by an excitation signal 52. This excitation signal is derived from a timing generator 12, which is in turn driven by an oscillator 10. This excitation signal
30 consists of a 1/16 duty cycle pulse which charges the capacitance of the sensor plates 24 and 32. The voltage 54 and 56 at the sensor plates 24 and 32 then rises exponentially and at some point reaches the upper voltage threshold 64 of the Schmitt triggers 20 and 28. The
35 change in logic level at the Schmitt triggers 20 and 28 outputs then drives the D type flip-flop 22 clock input 58 and data input 60 to determine which signal, clock 58 or

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data 60, arrived first. A null condition is then defined as the clock and data signals occurring at the same time. In actuality, these two signals do not occur "exactly" simultaneously but are very close at null, with a resolution determined by the least significant bit resolution of the D/A converter 36. The excitation signal 52 then goes to a "zero" for 15/16 of the excitation period allowing the capacitance of the sensor plates 20 and 28 to fully discharge.

10 The data input terminal of the averager 16 is connected to the D type flip-flop 22 output terminal. The averager 16 receives a 10 KHz clock signal from the timing generator 12. Therefore, every 100 microseconds, the averager 16 determines if the output of the flip-flop 22
15 is a one or a zero. There are two counters within the averager 16. One is a counter which counts to sixty-four, and starts over again once it reaches sixty-four. The other counter in the averager 16 is an accumulator counter, and is only incremented if the input from the
20 flip-flop 22 is a one. If the input from the flip-flop 22 is zero, the counter is not incremented. Therefore, at the end of sixty-four cycles, the accumulator counter in the averager 16 will have accumulated the number of times the output from the flip-flop 22 was one. If the
25 accumulator counter has accumulated less than 28 ones after sixty-four cycles, the output of the averager 16 is zero. If the accumulator counter has accumulated greater than 36 ones, the output of the averager 16 is one. Finally, if the count was between 28 and 36, then there is
30 no change in the output of the averager 16.

The advantage of this averager 16 is that the output of the averager is "crisp," i.e., the changes in the output from the flip-flop 22 which occur as a result of noise are eliminated. This is due to the noise area which
35 is centered around fifty percent (28 to 36 counts), in which the output of the averager does not change. So, as the noise is reduced from the output of the averager 16,

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the transition between the lighting of the LED's 26 is more smooth and precise. There is no wavering or flickering.

The display processor 18 receives the output of the 5 averager 16. The Display Processor 18 includes a 4 bit up counter, with decoded states 12 through 15 each enabling an individual latch and LED steering logic. Each of these four latches receives the output of averager 16 on their data inputs. Thus at the end of any averaging cycle 10 coinciding with states 12 through 15 of the counter, the data result is latched into the appropriate latch. The four outputs of the latches are used to enable the LED Display 26, with steering logic between the latch outputs and the LED drivers to allow for various device models.

15 The four bit output of the Display Processor 18 also drives the four bit input of the sensitivity select multiplexer 30 which in turn drives the five bit input of the Adder 34. During the calibration cycle, the counter of the Display Processor 18 is held in reset at state 11, 20 one state less than the lowest display LED at state 12. The unit also senses a decrease in density by adding a fifth latch at counter state 6 such that if a sensor null is detected at state 6 or below, this condition is signaled to the user.

25 In normal operation, with the unit calibrated at counter state 11 (assuming the unit was not calibrated over or near a stud), the sensor null state will occur at counter state 11 when not over a stud and as a stud is approached, the null state will progress to counter states 30 12 through 15, progressively lighting the display LED's 26.

If however, the unit was calibrated over a stud and then is moved laterally away from the stud, the null state will progress downward from counter state 11 until the 35 null is at counter state 6, signalling a sufficient decrease in density to signal the operator of an (erroneous) over-the-stud calibration situation.

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Counter state 6 is a compromise between still allowing normal operation if the unit was calibrated somewhat in proximity to a stud, which will still allow adequate sensing of a stud while still allowing small decreases in density from the calibrated condition due to wall texture, etc. and actually calibrating very close to or over a stud, which could prevent normal stud sensing.

The four bit output 33 from the Display Processor 18 is inputted into a sensitivity select multiplexer 30. The sensitivity select multiplexer 30 is controlled by the sensitivity mode control signal 31.

The sensitivity mode control signal 31 is either a one, for high sensitivity mode, or zero, for normal sensitivity mode. The user controls which mode the device operates in. When the power switch is pressed, the device is in normal sensitivity mode and the sensitivity mode control signal 31 is zero. Capacitive memory keeps track of when the device is turned on. This capacitive memory is accomplished by the specialized use of a bilateral port similar to that shown in FIG. 3. FIG. 4 shows one embodiment of this capacitive memory. During Power On Reset, which occurs during the first 50 microseconds after application of power, the charge on capacitor 40 is set into the latch 72. After Power On Reset has subsided and after the first sixteen clock pulses, the output driver 70 is enabled via the Enabling Signal. The state of the output level is then opposite that during Power On Reset due to the inverted Q output being fed to the output driver 70. The "memory" capacitor, 40, then charges or discharges to the opposite state prior to the Power On Reset cycle of the next power cycle, then sets the latch 72 to the opposite state.

The external capacitor/resistor values are chosen to retain a charge sufficient for logic level detection for about 2 to 3 seconds to allow the user to cycle the power switch and thus toggle the sensitivity of the unit between Normal and High. The unit always powers up in Normal

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sensitivity mode after being off for greater than 10 seconds. If the power switch is released and then repressed after the initial powering up of the device within a period of time determined by the capacitive 5 memory R-C time constant, the device enters high sensitivity mode and the sensitivity mode control signal 31 is one.

Thus depending upon the sensitivity mode control signal 31, the sensitivity select multiplexer receives the 10 four bit output 33 from the display processor and directs these four bits to either bits 1 thru 4 or bits 2 thru 5 of the five bit input of the adder 34. The unused bit (either bit 1 or 5) of the 5 bit input to the adder 34 is grounded.

15 A successive approximation register (SAR) 38 also receives the output from the averager 16. The SAR 38 does rapid A/D conversion, needing only 8 clock cycles (for 8 bits) to accomplish the conversion. The SAR 38 is generally coupled with some other D/A structure (the D/A 20 converter 36 in one embodiment), and produces an analog voltage based on its 8 bit input.

An eight bit adder 34 then receives the output from the display processor 18 via the sensitivity select multiplexer 30, and the output from the successive 25 approximation register 38, and sums them digitally. If the 8 bits of the successive approximation register 38 are referred to as bits 1 thru 8, in normal sensitivity mode, the four bits of the display processor 18 are only added to bits 2 thru 5 of the of the successive approximation 30 register 38. In high sensitivity mode, the four bits of the Display Processor 18 are added to bits 1 thru 4 of the successive approximation register 38. So, in high sensitivity mode, the least significant bit (LSB) from the Display Processor 18 is added to the LSB of the 5 bit 35 adder 34 input, causing each step of the Display Processor to step the D/A converter 36 by one bit.

In Normal sensitivity modes, the LSB from the Display

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Processor 18 is added to the second LSB of the adder 34, causing each Display Processor 18 step to step the D/A converter 36 by two bits, thus halving the sensitivity.

Calibration

5 When the unit is initially placed on a wall and then turned on, the counter in the display processor 18 is held at the calibrated value 1011 binary (11 decimal) and the unit determines the required offset injection voltage to the sensor circuit to produce a capacitive null of the two
10 sensor plates 24 and 32.

After the calibration cycle is complete, the unique 8 bit calibration word which corresponds to the required offset injection voltage is stored in the successive approximation register 38 and summed with the four bit
15 output 33 of the Display Processor counter 18 by the eight bit adder 36. Depending on the sensitivity required, the 4 bit output 33 is either summed with bits 1-4 or bits 2-5 of the 8 bit calibration word. The sensitivity is operator selectable through the sensitivity mode control 31.

20 If the user happens to calibrate the prior art device over a stud, when the device is moved away from the stud, the device has no response and will not sense studs. As the device is looking for an increase in density, and it has been calibrated where the wall is most dense, no
25 increase will be detected.

In accordance with another feature of the invention, the invention will sense both an increase and decrease in density. So, if the device is calibrated over a stud, and a density decrease is sensed, the operator is signalled
30 via the piezo electric tone transducer 14 and the LED display 26, that he has in fact calibrated over a stud, and should move the device and recalibrate.

Moreover, in the prior art, there is a capacitive leakage problem which invalidates the calibration after
35 45-60 seconds. In accordance with the present invention, the calibration will remain constant due to the all-

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digital design.

Finally, factory calibration is simply done by adjusting a potentiometer 27 while holding the 8 bit D/A converter 36 at a fixed value.

5 Bidirectional driver

Shown in FIG. 3 is a feature in accordance with invention for using IC pins such as pin 104 as a terminal for both an output signal and input signal. It is to be understood that in one embodiment, much of the circuitry of FIG. 1 is incorporated into a single custom integrated circuit. During power-on reset of this IC, the D type flip-flop 102 receives data input on its terminal D from the IC pin 104, with the Power On Reset signal enabling the latch 102. After Power On Reset has ceased, and after 15 16 clock cycles, a latch (not shown) is set whose output is an enabling signal which enables the outputs of all bilateral, tri-state ports including tri-state output buffer 100.

Various embodiments of the invention have been 20 described. The descriptions are intended to be illustrative, not limitative. Thus, it will be apparent to one skilled in the art that certain modifications may be made to the invention as described without departing from the scope of the claims set out below.

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I claim:

1. A portable device for locating a stud positioned behind a surface comprising:
 - a sensor for sensing additional capacitive loading caused by the stud and sending data signals when said additional capacitive loading is sensed;
 - an averager for receiving the data signals from said sensor and averaging them; and
 - a display processor for receiving the averaged data and in response providing an indication on a display.
2. A device as in Claim 1 further comprising:
 - a sensitivity select multiplexer for receiving data signals from said display processor, said sensitivity select multiplexer being controlled by a control signal;
 - a successive approximation register for receiving the averaged data from said averager; and
 - an adder for adding the outputs of said successive approximation register and said sensitivity select multiplexer, and sending the resulting added signal to said sensor;
 - wherein said sensitivity select multiplexer determines which of a lower or higher sensitivity mode is desired; and
 - wherein said successive approximation register does analog to digital conversion of the averaged data.
3. A device as in Claim 2 wherein said successive approximation register also stores a calibration word.
4. A device as in Claim 2 further comprising a digital-to-analog converter, wherein said converter converts said resulting added signal from a digital signal to an analog signal before providing the resulting signal

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to said sensor.

- 5 5. A device as in Claim 1 further comprising a timing generator for providing timing signals to said averager and display processor.
6. A device as in Claim 1 wherein said display comprises an indicator for indicating when said device has been calibrated over a stud.
- 10 7. A device as in Claim 1 further comprising a switch for operating the device in a lower or higher sensitivity mode and wherein said display comprises an indicator for indicating when said device is in said higher sensitivity mode.
- 15 8. A device as in Claim 1 wherein said display comprises an audible signal.
9. A device as in Claim 1 further comprising a means for determining and indicating when said surface is too dense or not dense enough for determining the position of a stud;
- 20 10. A device as in Claim 1 where said sensor comprises:
- a first capacitor plate;
- 25 a pair of second capacitor plates located one on each side of said first capacitor plate and in substantially the same plane as said first capacitor plate; and
- 30 a logic circuit for producing a data signal representative of the change in the relative capacitance between said first capacitor plate and said pair of second capacitive plates in response to said plates being moved along a surface.

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11. A method for determining the location of a stud positioned behind a surface comprising the steps of:

entering a first or second sensitivity mode under user control;

5 sensing the stud, wherein the step of sensing may occur in either the first or second sensitivity mode; and

indicating when said stud has been sensed.

12. A method for determining location of a stud 10 positioned behind a surface comprising the steps of:

providing a stud sensing device;

calibrating the device;

determining if said calibration has occurred over a stud; and

15 indicating by said device when said calibration has occurred over a stud.

13. A method for locating a stud positioned behind a surface comprising the steps of:

20 sensing additional capacitive loading caused by the stud;

sending data signals when said additional capacitive loading is sensed;

averaging said data signals over a predetermined time period; and

25 displaying said data signals.

14. A circuit for allowing both input to and output from a single terminal comprising:

a terminal;

30 a tri-state driver for receiving an input signal and providing an output signal to said terminal;

a flip-flop for receiving input signals from said terminal and providing an output signal;

wherein said tri-state driver is controlled by an enabling signal; and

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wherein said flip-flop is controlled by a clock signal.

15. The circuit of 14 wherein the circuit is a part of a portable device, and wherein the enabling signal is 5 generated when the device is powered on.

AMENDED CLAIMS

[received by the International Bureau on 29 November 1993 (29.11.93);
original claims 1,2,6,10,12,13 and 15 amended; new claims 16-25 added;
other claims unchanged (6 pages)]

1. A portable device for locating a stud positioned
behind a surface comprising:

5 a sensor for sensing additional capacitive
loading caused by the stud while said sensor moves
along the surface approaching the stud and sending
providing digital data signals as output when said
additional capacitive loading is sensed;

10 a digital an averager for receiving the data
signals from said sensor and averaging them; and
a display processor for receiving the averaged
data and in response providing an indication of the
stud position on a display unit.

2. A device as in Claim 1 further comprising:

15 a sensitivity select multiplexer for receiving
data signals from said display processor, said
sensitivity select multiplexer being controlled by a
control signal a state of which represents a low or
high sensitivity of the device;

20 a successive approximation register for
receiving the averaged data from said averager; and
an adder for adding the outputs of said
successive approximation register and said
sensitivity select multiplexer, and sending the
resulting added signal to said sensor;

25 wherein said sensitivity select multiplexer
provides said digital data signal as output in
response to a state of the control signal, and
provides another digital data signal as output in
response to another state of the control signal
30 determines which of a lower or higher sensitivity
mode is desired; and

wherein said successive approximation register
does analog to digital conversion of the averaged
data.

35 3. A device as in Claim 2 wherein said successive
approximation register also stores a calibration word.

4. A device as in Claim 2 further comprising a digital-to-analog converter, wherein said converter converts said resulting added signal from a digital signal to an analog signal before providing the resulting signal to said sensor.

5. A device as in Claim 1 further comprising a timing generator for providing timing signals to said averager and display processor.

6. A device as in Claim 1 wherein said display unit comprises an indicator indicating when said device has been calibrated over a stud.

7. A device as in Claim 1 further comprising a switch for operating the device in a lower or higher sensitivity mode and wherein said display comprises an indicator for indicating when said device is in said higher sensitivity mode.

8. A device as in Claim 1 wherein said display comprises an audible signal.

9. A device as in Claim 1 further comprising a means for determining and indicating when said surface is too dense or not dense enough for determining the position of a stud.

10. A device as in Claim 1 where said sensor comprises:

- 25 a first capacitor plate;
- a pair of second capacitor plates located one on each side of said first capacitor plate and in substantially the same plane as said first capacitor plate; and
- 30 a logic circuit for producing a digital data signal representative of the change in the relative capacitance between said first capacitor plate and said pair of second capacitive plates in response to

said plates being moved along a said surface.

11. A method for determining the location of a stud positioned behind a surface comprising the steps of:

- entering a first or second sensitivity mode
- 5 under user control;
- sensing the stud, wherein the step of sensing may occur in either the first or second sensitivity mode; and
- indicating when said stud has been sensed.

10 12. Amended A method for determining location of a stud positioned behind a surface comprising the steps of:

- providing a stud sensing device sensing additional capacitive loading caused by the stud when the device moves along the surface approaching the
- 15 stud;
- calibrating the device;
- determining by sensing decreasing of the capacitive loading if said calibration has occurred over a stud; and
- 20 indicating by said device when said calibration has occurred over a stud.

13. A method for locating a stud positioned behind a surface comprising the steps of:

- sensing additional capacitive loading caused by
- 25 the stud while a sensor moves along the surface approaching the stud;
- sending digital data signals when said additional capacitive loading is sensed;
- averaging said data signals digitally over a
- 30 predetermined time period; and
- displaying said data signals.

14. A circuit for allowing both input to and output from a single terminal comprising:

- a terminal;
- 35 a tri-state driver for receiving an input signal

and providing an output signal to said terminal;
a flip-flop for receiving input signals from
said terminal and providing an output signal;
wherein said tri-state driver is controlled by
5 an enabling signal; and
wherein said flip-flop is controlled by a clock
signal.

15. The circuit of Claim 14, wherein the circuit is
a part of a portable device, and wherein during a power-
10 on-reset period, the tri-state driver is in a tri-state
and the flip-flop is enabled to latch the input signal
from the terminal the enabling signal is generated when
the device is powered on.

16. A device as in Claim 1, further comprising means
15 for setting the sensor to operate in a first or second
sensitivity mode under user control.

17. A device as in Claim 1, further comprising means
in response to decreasing of capacitive loading sensed by
the sensor for indicating when the device has been
20 calibrated when located over a stud.

18. A portable device for locating a stud positioned
behind a surface comprising:

a sensor circuitry including a differential
capacitive plate circuit, sensing unbalanced
25 capacitive loading of two plates in the differential
capacitive plate circuit, and providing digital data
signals when unbalanced capacitive loading of the two
plates is sensed; and

a display processor receiving said digital data
30 signals and in response providing an indication of
the stud position on a display, said display
processor providing a linearly stepped voltage to
said differential capacitive plate circuit as an
offset voltage to cause the sensor circuitry to a
35 null state.

19. A device as in Claim 18 further comprising a sensitivity select circuit receiving said linearly stepped voltage and a control signal the state of which is indicative of a low or high sensitivity, and providing as
5 output said linearly stepped voltage in response to one state of the control signal and another linearly stepped voltage in response to another state of the control signal.

20. A device as in Claim 18 further comprising a
10 register restoring a data signal representing an initial offset voltage to cause the sensor circuitry to the null state when the device is calibrated.

21. A device as in Claim 20 wherein a sum of said initial offset voltage and said output of the sensitivity
15 select circuit forms said offset voltage to the differential capacitive plate circuit.

22. A device as in Claim 20 further comprising a digital adder receiving as two input data, the data signal stored in the register and a data signal representing said
20 output of the sensitivity select circuit, and a digital-to-analog converter converting a sum data signal from the digital adder to an analog voltage as said offset voltage to the differential capacitive plate circuit.

23. A device as in Claim 1, wherein said data
25 signals are in an asserted state when said additional capacitive loading is sensed and wherein said digital averager samples said data signals at a preset time period for a predetermined interval and at the end of the interval provides an digital output signal at said
30 asserted state when a number of the sampled data signals of being at the asserted state exceeds a first predetermined number, and provides the output signal at a deasserted state when the number of the sampled data signals of being at the asserted state is less than a
35 second predetermined number, and otherwise remains an

output signal provided at the end of the previous interval as the output thereof.

24. A device as in Claim 23, wherein said averager comprises a first counter which counts a clock signal
5 having a cycle of said preset time period and starts counting over again once the counts thereof reaches a preset number corresponding to said predetermined interval, and a second counter which counts said clock
10 signal only when said data signals are in said asserted state, and a comparison logic comparing the counts of said second counter when said first counter reaches said preset number with said first and second predetermined number and providing the averaged data at one of the asserted and deasserted state.

15 25. A method as in Claim 13, wherein said step of averaging comprises the steps of:

sampling said digital data signals at
a preset time period counting a number of
sampled data signals of being at an asserted state over
20 the predetermined time period; and

providing at the end of the predetermined time
period a digital output signal at said asserted state
when the counted number exceeds a first predetermined
number, and providing the digital output signal at a
25 deasserted state when the counted number is less than
a second predetermined number, and otherwise
providing a digital output signal thereof provided at
the end of the previous predetermined time period as
output.

STATEMENT UNDER ARTICLE 19

Amended Claims 1, 2, 6, 10, 12, 13, and 15, and new Claims 16 - 26 submitted in the "Letter under PCT Rule 46.5" recite alternative embodiments of Applicant's invention as described in the Applicant's specification. Since each of amended and added Claims is supported by Applicant's specification and drawings, the amended and added claims have no effect upon the specification and drawings. Claims 1, 2, 6, 10, 12, 13 and 15, as well as Claims 16 - 26 more clearly recite Applicant's invention and more particularly distinguish over the cited references in the international search report of October 1, 1993, regarding the above application.

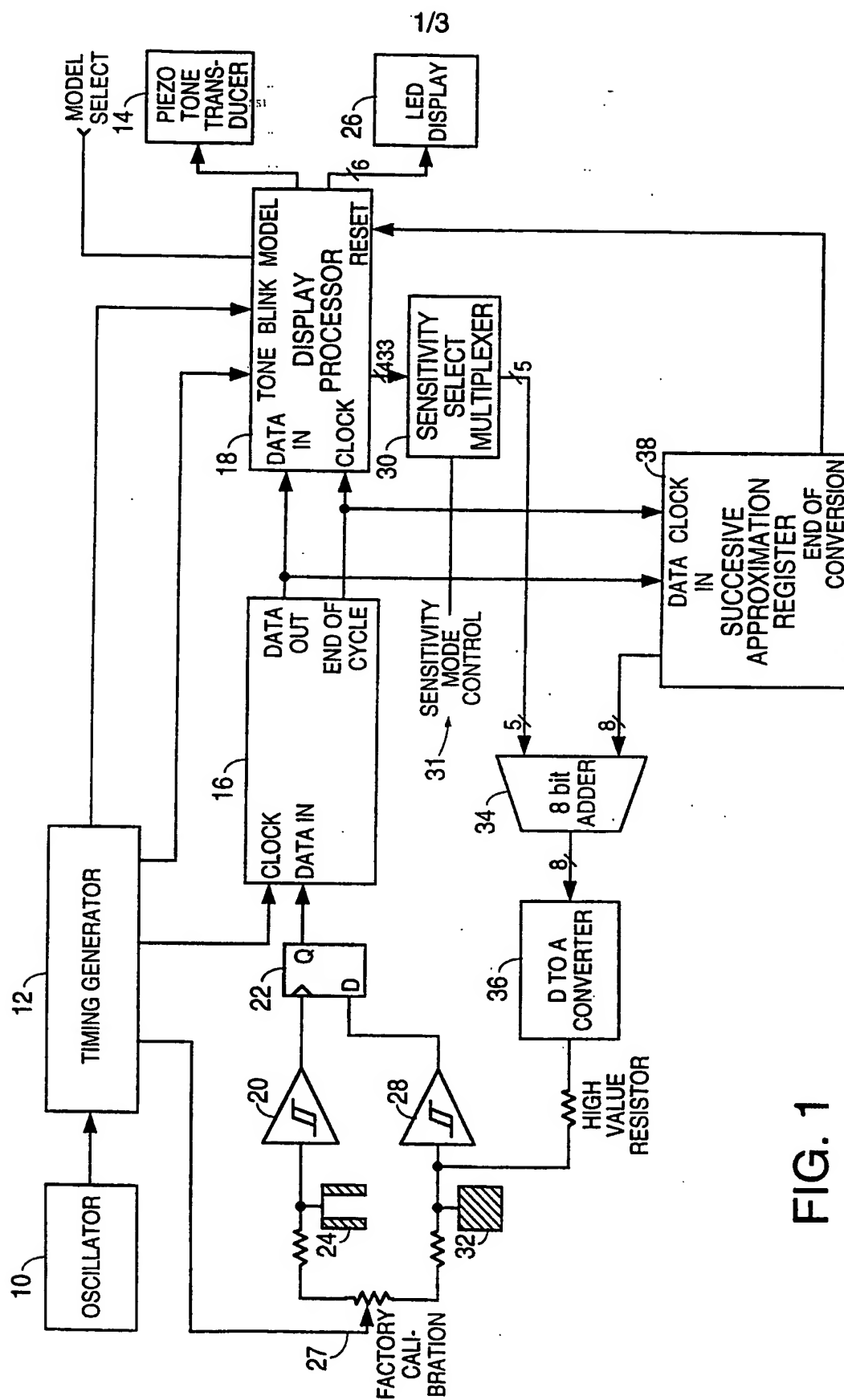


FIG. 1

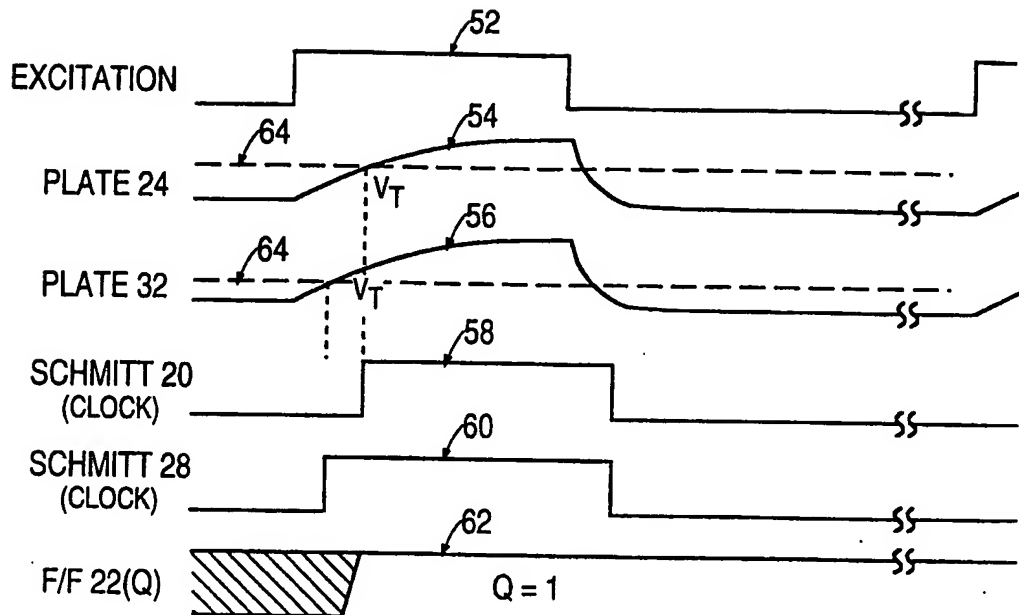


FIG. 2

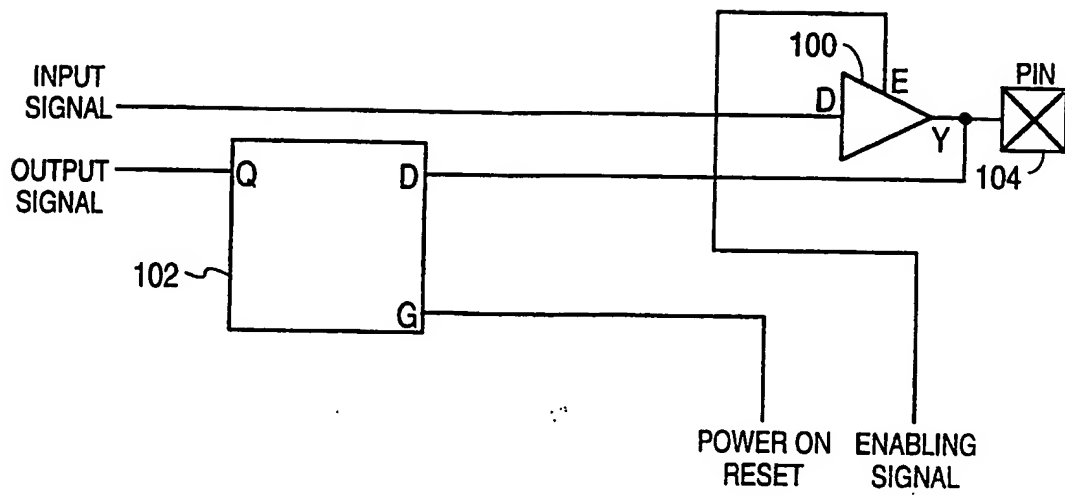


FIG. 3

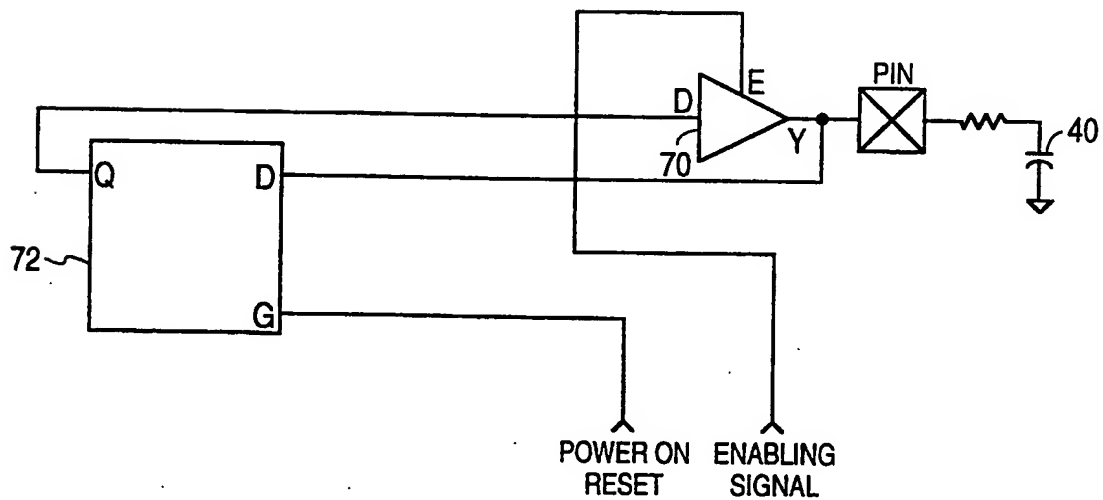


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/07433

A. CLASSIFICATION OF SUBJECT MATTER

IPC(S) : G01R 19/00; H30K 19/00; G01R 35/00

US CL : 324/67, 601; 307/465, 473

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 324/66, 67, 326, 601, 658, 662, 663, 671, 672, 676, 686, 690; 307/465, 473, 519, 296.1, 296.3.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---- Y ---- A	US, A, 4,46422 (Franklin) 07 August 1984, see entire document.	1, 5, 9, 10, 13 ----- 6, 7, 8 ----- 2 - 4
X ---- Y A	US, A, 5,023,484 (Pathak et al) 11 June 1991, see Figure 1.	14 ----- 15
A	US, A, 4,939,455 (Tsugawa) 03 July 1990, see Figure 2.	14, 15
A	US, A, 4,947,116 (Welcome et al) 07 August 1990, see Figure 4.	14, 15

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be part of particular relevance	*X*	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	*Y*	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Z*	document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means		
P document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

17 September 1993

Date of mailing of the international search report

01 OCT 1993

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. NOT APPLICABLE

Authorized officer

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/07433

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A 4,322,678 (Capots et al) 30 March 1982, see col. 6, line 30, et seq.	1-10,13
A	US, A, 3,278,843 (Deming) 11 October 1966, see entire document.	1-13
A	US, A, 4,086,528 (Walton) 25 April 1978, see entire document.	1-13
A	US, A, 4,853,617 (Douglas et al) 01 August 1989, see entire document.	1-13
A	US, A, 4,992,741 (Douglas et al) 12 February 1991, see entire document.	1-13
A	US, A, 4,676,100 (Eichberger) 30 June 1987, see Figure 2.	12
X	US, A, 4,041,382 (Washburn) 09 August 1977, see Figure 2, and entire document.	11
A		12
X	US, A, 4,067,225 (Dorman et al) 10 January 1978, see abstract.	12
X	US, A, 4,130,796 (Shum) 19 December 1978, see abstract, Figure 1.	12

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US93/07433

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Telephone Practice

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐

The additional search fees were accompanied by the applicant's protest.

☐

No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/07433

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING

This ISA found multiple inventions as follows:

- I. Claims 1-10, and 13, drawn to an apparatus and method for locating a stud positioned behind a surface by capacitive loading classified in class 324, subclass 67.
- II. Claim 11, drawn to a method for locating a stud positioned behind a surface by selecting sensitivity modes classified in class 324, subclass 67.
- III. Claim 12, drawn to a method for calibrating a stud sensing device classified in class 324, subclass 67.
- IV. Claims 14 and 15, drawn to a single input/output terminal classified in class 307, subclass 473.